## REMARKS

In the outstanding Office Action, the Examiner rejected claim 25 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 5,424,245 to Gurtler et al. ("Gurtler") in view of U.S. Patent No. 5,977,640 to Bertin et al. ("Bertin"). By this amendment, Applicant has amended claim 25. Claims 1, 2, 4-11, 14-18 and 25 are pending in this application, with claim 25 presented for examination.

Applicant respectfully traverses the rejection of claim 25 under 35 U.S.C. § 103(a).

To establish a *prima facie* case of obviousness under 35 U.S.C. § 103(a), each of three requirements must be met. First, the reference or references, taken alone or combined, must teach or suggest each and every element recited in the claims. Second, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to combine the references in a manner resulting in the claimed invention. Third, a reasonable expectation of success must exist. Moreover, each of the three requirements must " be found in the prior art, and not be based on applicant's disclosure. " *See* MPEP § 2143, 8th Ed. (Rev. 4), October, 2005. At a minimum, the Examiner has failed to establish a *prima facie* case of obviousness because the references, whether taken alone or in combination, fail to teach or suggest each and every element recited in claim 25.

For example, claim 25, as amended, recites a combination including "a second semiconductor chip stacked on the first semiconductor chip and having a heat radiating

plate and a radiating resin formed thereon, the radiating resin affixing the heat radiating plate to the second semiconductor chip." The Examiner asserts that "Gurtler shows the most aspect[s] of the instant invention except having a larger second semiconductor chip and a heat radiating plate thereon." Office Action, page 3. As acknowledged by the Examiner, Gurtler fails to teach or suggest "a heat radiating plate," and thus also fails to teach or suggest "a radiating resin formed [on the heat radiating plate]," as also recited in claim 25. Moreover, Gurtler is silent as to "a radiating resin." Gurtler thus fails to teach or suggest a combination including "a second semiconductor chip stacked on the first semiconductor chip and having a heat radiating plate and a radiating resin formed thereon, the radiating resin affixing the heat radiating plate to the second semiconductor chip," as recited in claim 25 (emphasis added).

Bertin fails to cure the deficiencies of Gurtler. The Examiner alleges that "Bertin shows a multi-chip packaging device wherein the second semiconductor chip (30) is larger than the first semiconductor chip (40) and a heat radiating plate (74) [is formed] thereon." Office Action, page 3. Bertin teaches "heatspreader 74 is connected to the first chip 30 through an adhesive 78 ... allow[ing] for heat dissipation for chip-on-chip component 10B." Bertin, col. 4, lines 16-19. Even if heatspreader 74 can be reasonably construed as corresponding to Applicant's claimed "heat radiating plate," Bertin is silent as to a radiating resin, and thus fails to teach or suggest "[a] radiating resin affixing the heat radiating plate to the second semiconductor chip," as recited in claim 25 (emphasis added). Accordingly, a *prima facie* case of obviousness has not been established with respect to claim 25.

Moreover, Applicant notes that claim 25 further recites a combination including "a plurality of conductive members buried in a plurality of through holes that extend through the first semiconductor chip." Since "a plurality of through holes" are made to "extend through the first semiconductor chip," the first semiconductor chip is weakened, and may easily be cracked or broken. Claim 25, however, further recites that "a second semiconductor chip [is] stacked on the first semiconductor chip," wherein "the second semiconductor chip is thicker than the first semiconductor chip." Thus, the claimed "second semiconductor chip" may physically reinforce the claimed "first semiconductor chip."

The above-described reinforcement feature of the claimed "second semiconductor chip" provides another advantage that it allows the claimed "plurality of through holes that extend through the first semiconductor chip" to be made thin. It is desirable in view of the electric performance of the semiconductor device to make the first semiconductor chip thin. To be specific, the claimed "through holes" extending through the first semiconductor chip brings about dielectric loss, which may degrade the electric performance of the semiconductor device. To reduce the dielectric loss, it is desirable to make the length of the claimed "through holes" extending through the first semiconductor chip, and thus the thickness of the first semiconductor chip, as small as possible. Thus, the claimed "second semiconductor chip stacked on the first semiconductor chip," wherein "the second semiconductor chip is larger than the first semiconductor chip," allows the reinforcement of the claimed "first semiconductor chip."

This provides a high electrical performance to the semiconductor device. Accordingly, claim 25 is also allowable for at least this reason.

In view of the foregoing remarks, Applicant requests the reconsideration and reexamination of the application, and the timely allowance of the pending claims.

Please grant any extensions of time required to enter this response and charge any additional required fees to our deposit account 06-0916.

Respectfully submitted,

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